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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,699	01/26/2001	F. Daniel Gealy	98093DIV	7854

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,699	GEALY ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-43,45-49 and 52-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-43,45-49,52-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on September 17, 2004. Claims 38-43,45-49,52-60 are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim rejections - 35 USC § 103

1. Claims 38-43,45-49,52-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi et al (6,222,722) taken with Chen et al (6,077,742) and Agarwal et al (6,165,834) and

Fukuzumi et al teaches a method for forming a capacitor comprising at least the steps of: forming on a substrate assembly; forming a layer of hemispherical grain polysilicon (re claims 52,58; 12 in Fig 11; col 9, line 45 through col 10; 51 in Figs 30-34; col 14, line 45 through col 15) in a recess of a substrate assembly including the layer (10 in Fig 11; 21/20 in Figs 22,27-29) and the layer (2 in Figs 11,22; 20/38 in Figs 27-29), wherein a portion of the substrate assembly is removed; forming a first electrode 13,24,52 on the hemispherical grain polysilicon recessed in the substrate assembly, wherein the first electrode 13,24,52 is selected from the group consisting of transition metal or a conductive metal oxide (13 in Fig 12; col 7, lines 40-60; 24 in Figs 27-29; or 52 in Figs 30-34); removing the hemispherical grain polysilicon 23,4 (Figs 22-23,4-5); forming a dielectric 14,26,53 on the first electrode, wherein the first electrode extends above an uppermost surface of a substrate assembly including the insulating interlayer (20 in Figs 27-29; or 66/10 in Fig 38), the insulating layer 2 and an interconnect 3 recessed in the assembly (Figs 6,24,26,27-29,38); and forming a second electrode (15 in Fig 13; 27 in Fig 29, 54 in Fig 33) having strap on the dielectric, wherein the dielectric is formed between the first and second electrodes, and wherein the first and second electrodes each include a non-smooth surface (Figs 13,29,33,34,38). Re claims 41-43,45, wherein the first electrode 13,24,52 of metal includes ruthenium, platinum, Ir, Rh and its metal oxide including RuO_2, wherein x = 2 (col 14, line 66 through col 15, line 10; col 9, lines 49-67; col 16, line 62 through col 7; col 20, lines 10-25), and wherein the second electrode 15,27,54 includes ruthenium, platinum, wherein material for forming the electrode including ruthenium, platinum, oxide thereof, or W, WN, Al, Ti, TaN (col 17, lines 12-18). Re claims 39-40,53-55, wherein forming the first electrode includes chemical vapor deposition (CVD) and planarization thereafter by CMP (13 in Fig 12; col 7, lines 40-60;

24 in Figs 22-23, col 11, line 65 through col 12; or 52 in Figs 30-34) on the hemispherical grain polysilicon. Re claims 46, wherein the second electrode 9,13,27,54 is formed by chemical vapor deposition (CVD) (col 8, lines 15-18). Re claims 47-48, wherein the dielectric 14,53 of an insulating metal oxide includes barium strontium titanate (BSTO), Ta_2O_5, $SrTiO_3$, $BaSrTiO_3$ (col; 17, lines 3-10). Re claim 56, wherein removing the hemispherical grain polysilicon 23,4 is shown in Figs 22-23,4-5. Re claims 49,57, wherein the substrate assembly is formed before forming the first electrode 13,24,52 (Figs 9-13,21-24,30-33). Re claim 59, the method includes forming an interconnect 3 recessed in the substrate assembly, wherein the first electrode 13,24,52 is formed in the interconnection recessed in the substrate assembly (Figs 1-5,21-24,33,38). Re claim 60, the method includes forming a contact 3 in the substrate assembly (Figs 21-24,33,38), and wherein the first electrode 13,24,52 is formed in the contact in the substrate assembly.

Fukuzumi already teaches forming the dielectric (8,14,26,53) on the first electrode (7,13,24,52) and on the uppermost surface of the substrate assembly 2, but lacks forming the second electrode (9,15,27,54) on the uppermost surface of the substrate assembly.

However, Chen teaches (at Figs 5-8; col 8, line 35 through col 9) forming a first electrode 36' in a recess of a substrate assembly and extending above the uppermost surface of the substrate assembly including an insulating layer 32/28 (Fig 5); forming a capacitor dielectric 40 on the first electrode 36' and the uppermost surface of the substrate assembly including the insulating layer 32/28; and forming the second electrode 42 on the dielectric 40 and the uppermost surface of the substrate assembly including the insulating layer 32/28. Agarwal teaches (a first embodiment at Figures 3-4) forming a first planar capacitor having the second electrode 30/28 formed on the dielectric 26 formed on the first electrode 24 and the uppermost surface of the substrate assembly 16. Agarwal then teaches (a second embodiment at Figure 5) forming a second capacitor in trench by forming the capacitor dielectric 40 at the selected portion of the substrate, on the first electrode 38, and on an uppermost surface of the substrate assembly, and forming the second electrode 42 on the dielectric 40 and the uppermost surface of the substrate assembly.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor of Fukuzumi by forming the capacitor dielectric layer on the first electrode, and forming the second electrode (9,15,27,54) entirely on the capacitor

dielectric layer and on the uppermost surface of the substrate assembly, as disclosed by Chen and Agarwal. This is also because of the desirability to complete and facilitate the next level of electrical interconnections in forming an electrical contact to the second electrode 42 that is laterally extended from the first electrode, and formed on the uppermost surface of the substrate assembly including the insulating layer 32/28 (Chen, Fig 8; col 9, lines 55 through col 10, line 4). Furthermore, this is also because of the desirability to form the top second electrode to entirely cover the capacitor dielectric layer, as shown in Figure 5 of Agarwal, wherein the trench capacitor has a planar structure, and wherein there is no high step formed due to patterning both of the second electrode and the dielectric layer.

Re further claims 41-43,45,58, Fukuzumi already teaches several alternative materials for forming the electrodes or the dielectric, but does not list all materials as claimed. Indeed, as applied above to claims 38-43,45-49,52-57, Fukuzumi teaches a method for forming a capacitor, wherein the first electrode 13,52 of metal includes ruthenium, platinum, Ir, Rh, and its metal oxide including RuO_2, wherein x = 2 (col 14, line 66 through col 15, line 10; col 9, lines 49-67; col 16, line 62 through col 7; col 20, lines 10-25), wherein the second electrode 15,54 includes ruthenium, platinum, wherein materials for forming the electrode include ruthenium, platinum, oxide thereof, or W, WN, Al, Ti, TaN (col 17, lines 12-18), wherein the dielectric 14,53 includes barium strontium titanate (BST), Ta_2O_5, $SrTiO_3$, $BaSrTiO_3$ (col; 17, lines 3-10). Agarwal further teaches forming the dielectric between the first and second electrodes, wherein the metal oxide includes CVD Ruthenium dioxide, RuO_2, wherein x = 2, wherein the second capacitor electrode includes Platinum, TiN, Ru, WN, IrO, RuO, Pt, Ir, polysilicon (col 3, lines 42-45; col 5, lines 1-7), wherein the dielectric 40,26 includes barium strontium titanate (BST), $SrTiO_3$, (Ba, $Sr)TiO_3$, Ta_2O_5 (col 3, lines 55-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrodes or the dielectric of Fukuzumi by using other alternative materials as well known in the semiconductor art and as combinatively taught by Fukuzumi and Agarwal. This is because the substitution of art recognized equivalent materials would have been obvious and within the level of ordinary skill in the semiconductor art, wherein these dielectric materials are having high dielectric constant, and wherein these conductive materials are oxidation barrier and having high electrical conductivity. Re further claim 40,

planarization after CVD forming the first electrode is taught by Fukuzumi (at Fig 4; col 7, lines 40-59), because of the desirability to isolate a plurality of lower electrodes one from each other, and to form stacked container capacitor having high capacitance.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

3. Claims 38-43,45-49,52-60 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 81-112 of U.S. Application Serial No. 10/172,253; Claims 81-113 of Application Serial No. 10/299,145, Claims 81-109 of U.S. Application Serial No. 10/299,752; and Claims 81-108 of U.S. Application Serial No. 10/299,728 . Although the conflicting claims are not identical, they are not patentably distinct from each other, because claim 38 of this present application differs from, for example, claim 81 of the 10/172,253 application in that the first electrode extends above an uppermost surface of the substrate assembly. However, forming the first electrode extends above the uppermost surface of the substrate assembly would have been obvious to one of ordinary skill in the art as taught by Prall (5,866,453) or Fukuzumi, because of the desirability to expose more surface of the capacitor electrodes so as to increase capacitance of the capacitor. Additionally, Kim (6,090,704; see Figure 3F) teaches forming an additional substrate oxide layer 118 having an opening, and forming in the opening an interconnect 124 for electrically connecting to the second electrode 112. Thus, it would have been obvious to one of ordinary skill in the art to

complete fabrication of a capacitor of Fukuzumi (6,222,722; see Figure 29) by providing an interconnect through the opening formed in the second substrate oxide layer to connect to the second electrode. This is because of the desirability and necessary to provide electrical connection to the second electrode so that the device can be properly operated. Furthermore, forming the first and second electrodes having a non-smooth surface would have been obvious as taught by Fukuzumi, since it would increase the capacitor plate area. Furthermore, Chu et al (5,856,937) teach forming a computer system having processors including capacitor and memory devices including capacitors, wherein the first device and second device are connected via a bus (at col 10, lines 20-65; col 1, lines 16-67; Figs 2-4; col 6-8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the capacitor as made by Fukuzumi to form a computer system having processors and memory devices as taught by Chu et al. This is because of the desirability to form a computer system for storing and processing information, wherein the processors having capacitors are central processing unit for processing data for operation, and wherein the memory devices having capacitors are used for accessing data stored in the capacitors.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b), and be timely submitted.

Response to Amendment

4. Applicant's remarks filed September 17, 2004 with respect to the claims have been considered, but they are moot in view of the new ground(s) of rejection.

First, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

In response to Applicant's analysis of the references, the rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another reference. In Re Lyons 150 USPQ 741 (CCPA 1966). Moreover, it is

well settled that one can not show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. In Re Keller, 208 USPQ 871 (CCPA 1981); In Re Young, 159 USPQ 725 (CCPA 1968).

Applicant remarked that Chen is silent to form the second electrode having at least one non-smooth surface as recited in base claims 38,52,58.

In response, this is noted and found unconvincing. First, as clearly shown in Figure 8 of Chen (6,077,742), the second electrode 42 is having a non-smooth surface adjacent to the capacitor dielectric layer 40. Furthermore, the first electrode 36', the second electrode 42, and the capacitor dielectric layer 40 are all having at least one non-smooth surface. Second, under 35 USC 103 rejection, the primary reference of Fukuzumi already teaches forming the first (7,13,24,52) and second electrode (e.g. 9,15,27,54) having at least one non-smooth surface, wherein forming the second electrode entirely on the capacitor dielectric layer and on the uppermost surface of the substrate assembly are taught by the references and would have been obvious to one of ordinary skill in the art, as taught by Chen and Agarwal. This is because of the desirability to complete and facilitate the next level of electrical interconnections in forming an electrical contact to the second electrode 42 that is laterally extended from the first electrode, and formed on the uppermost surface of the substrate assembly including the insulating layer 32/28 (Chen, Fig 8; col 9, lines 55 through col 10, line 4). This is also because of the desirability to form the top second electrode to entirely cover the capacitor dielectric layer, as shown in Figure 5 of Agarwal, wherein a planar trench capacitor having a planar structure is formed, and wherein there is no high step due to patterning both of the second electrode and dielectric. Under 35 USC 103 rejections, forming the first electrode in a recess of the substrate assembly and extending above the uppermost surface of the substrate assembly, and forming the second electrode on the dielectric and on the uppermost surface of the substrate assembly are taught by the references and would have been obvious to one of ordinary skill in the art so that the first electrode is formed in a recess opening of a substrate assembly contacting the underlying conductive layer for electrically connection.

The Examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. IN re McLaughlin 170 USPQ 209 (CCPA 1971): IN Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one

versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

The prior art motivation or advantage may be different than that of applicant while still supporting a conclusion of obviousness. In Re Wiseman 201 USPQ 658 (CCPA 1979); Ex Parte Obiaya 227 USPQ 58 (Bd. of App. 1985).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-6

Michael Trinh
Primary Examiner